# Digital Beamforming for Mobile Devices

## The Power Efficient Architecture for 5G on mmWave Frequencies

## Executive Summary

Currently the 5th cellular network generation, 5G-New Radio (NR), is emerging worldwide, enabling new wireless services requiring ultra-low latency and Gbit/s data rates using the millimeter Wave (mmWave) frequency bands, 24 GHz and above.

The high isotropic path loss in the millimeter Wave (mmWave) frequency band makes it necessary to use a large number of antenna elements. These antenna arrays overcome the path loss by high directional gain through beamforming. Thus, a transmitter-receiver pair uses many antennas to focus energy in a particular direction in order to mitigate the high path loss in the mmWave frequency band.

The optimal way to perform beamforming is to use a digital beamforming architecture, where each antenna element has its own transceiver chain and the beamforming is done in the digital baseband. Such an architecture has however been believed to be too power consuming for mobile device mmWave implementations. Therefore, current mobile device implementations use analog beamforming where the beamforming is performed in the analog domain and hence only requiring a single transceiver from the mixer stage down to digital baseband.

In this paper we show that with current state-of-the-art RF and Analog to Digital/Digital to Analog converter (ADC/DAC) technologies, as presented in [2]-[8], the power consumption for a digital beamforming architecture, when integrating antennas, front-end filters and radio transceiver in a single RF chip, is at least on par with analog beamforming implementations. In a typical use case of 70% downlink data and 30% uplink data, the digital beamforming solution has lower power consumption compared to analog beamforming architectures currently implemented in mmWave 5G mobile devices.

The reason for this, maybe at a first glance quite surprising result, is twofold. First, the insertion loss in the phase shifters and power combiners/splitters in the front-end radio increases the front-end power consumption for analog beamforming. Second, the digital beamforming requires $1.7\log10(N_{antenna})$ fewer bits in the converters, due to the inherent quantization noise suppression ability in the digital beamforming architecture, thereby reducing the ADC/DAC power consumption for the digital solution.

The power consumption advantages for digital beamforming architectures together with all other advantages in terms of performance, cost, size, and flexibility from a PCB design point-of-view, as discussed in [10], shows that a digital beamforming architecture where the RF IC, front end radio modules, filters, and antenna element are integrated in a single RF chip is the radio architecture that will enable the mass market for 5G-NR devices on mmWave radio frequencies.

## 5G-NR and mmWave

Currently the 5th cellular network generation, 5G-NR, is emerging worldwide, enabling new wireless services requiring ultra-low latency and Gbit/s data rates over the radio interface. Examples of such services may be autonomous driving, eHealth services like telesurgery, and portable Virtual or Augmented Reality systems.

5G-NR will enable an increase of capacity in frequency bands used for 3G and 4G today, i.e. radio frequencies below 6 GHz. Data rates are limited to some 100th of Mbit/s in these frequency bands. Therefore, services requiring the ultra-low latency and Gbit/s-rates new frequency bands currently not used for 3G and 4G will be enabled. These bands between 30-300 GHz are called mmWave bands, due to the radio signal wavelength being in the range of 10-1 mm. The first mmWave frequency bands that will be used in 5G-NR is the 28 and 39 GHz band [1]. It is however expected that other mmWave frequency bands will be utilized in the further development of 5G-NR.

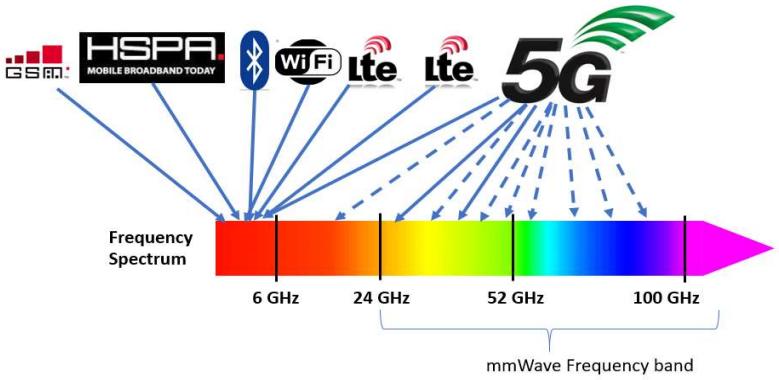


***Figure 1.*** *Radio spectrum used for different wireless communication technologies. The 5G-NR standard will be supported both in frequency bands used for 3G-HSPA and 4G-LTE today (below 6 GHz), but also in new frequency bands in the mmWave frequency range (24 GHz and higher).*

## The mmWave frequency band

The main advantage of using mmWave frequencies for cellular communication, is the large blocks of contiguous radio spectrum available and therefore overcome the bandwidth crunch problem at sub 6 GHz frequency bands. Furthermore, the short wavelength for mmWave making radio transceiver antennas can be made very small which is a major advantage for mobile smartphones and other mobile devices where size really matters.

However, the high isotropic path loss between the radio transmitter and radio receiver in the mmWave frequency band makes it necessary to use a large number of antenna elements to perform communication. These antenna arrays overcome the path loss by high directional gain through beamforming. Thus, a transmitter-receiver pair uses many antennas to focus energy in a particular direction in order to mitigate the high path loss in the mmWave frequency band, as shown in figure 2.

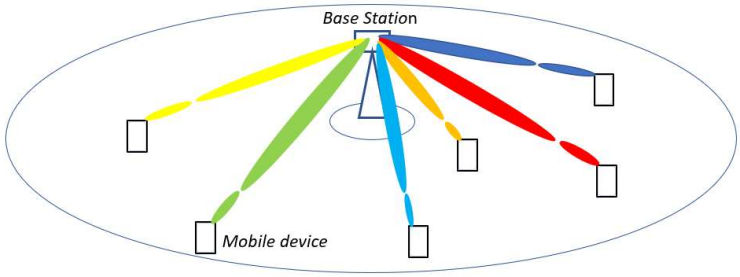


***Figure 2.*** *The principles behind Beamforming applied to a cellular communication system, such as 5G-NR. A base station – mobile device communicates via directing the radio signal towards each other using many antenna elements at both transceiver sides. A typical number of antenna elements for mmWave communication in 5G could be 64-256 antenna elements in a radio base station and 4-16 antenna elements in a mobile device.*

## Beamforming techniques – Analog vs Digital Beamforming

Beamforming of radio signals has found numerous applications in radar, radio astronomy and wireless communications. Radio implementations of beamforming can be based on a fully analog, fully digital beamforming or a combination, called hybrid beamforming.

Traditionally, mmWave implementations use analog beamforming. In this case, beamforming is performed at the radio frequency (RF) through a bank of phase shifters, one per antenna element, and an analog power combiner (receiver) and power splitter (transmitter), as shown in figure 3. This architecture only requires one pair of down- and up-converting mixers and analog-to-digital converters (ADC) and digital-to-analog converters (DAC) at the receiver and transmitter, respectively, reducing the complexity. The antenna elements are typically clustered and implemented in an antenna panel.

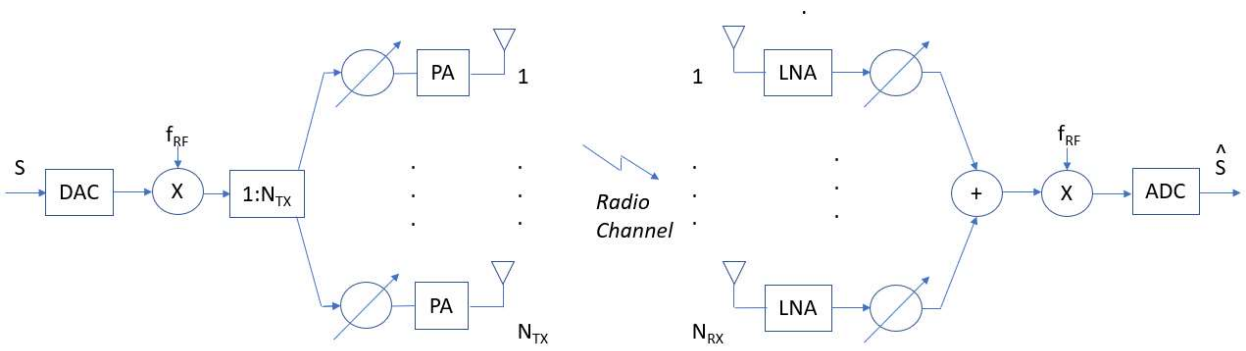


***Figure 3****. Analog beamforming radio architecture. After the DAC the transmitted baseband signal S is converted to a radio signal in a single up-conversion mixer and thereafter split in a power splitter and fed to a bank of phase shifters that are used for performing beamforming (left). At the receiver side (right) the respective received signal is fed to a phase shifter and the beamformed received signals are combined and then down-converted in a single mixer to a baseband signal prior to the ADC. This architecture uses just one pair of up and down converting and ADC and DAC at the baseband.*

While analog beamforming is believed to be power efficient, they are only capable of transmitting in one direction at a given time, which limits the potential of using beamforming. For instance, the tracking abilities of transmission direction is degraded in case the mobile device is moving fast relative to the radio base station when using analog beamforming, which may cause quality of service degradation (“lagging”) for services requiring ultra-low latency and high data rates. Furthermore, due to uncertainties in the phase

shifters as well as limited dynamic and resolution in the phase shifter settings, there is also a performance loss in stationary cases compared to the beamforming using ideal phase shifters.

In contrast, a digital beamforming architecture performs the beamforming in the digital baseband processor, see figure 4. Each transceiver chain has a pair of down-converting mixers and ADCs at the receiver and DACs and up-converting mixers at the transmitter, enabling the transceiver to simultaneously direct beams in theoretically infinite number of directions at a given time. Hence, digital beamforming architectures are much better at tracking radio signals when mobile devices move fast relative to the radio base station. Furthermore, since the beamforming is made in the digital domain, optimal beamforming (pre-coders) can be achieved much easier, without implementation losses, compared to analog beamforming, and hence also in the stationary case, digital beamforming is in favor over analog beamforming.

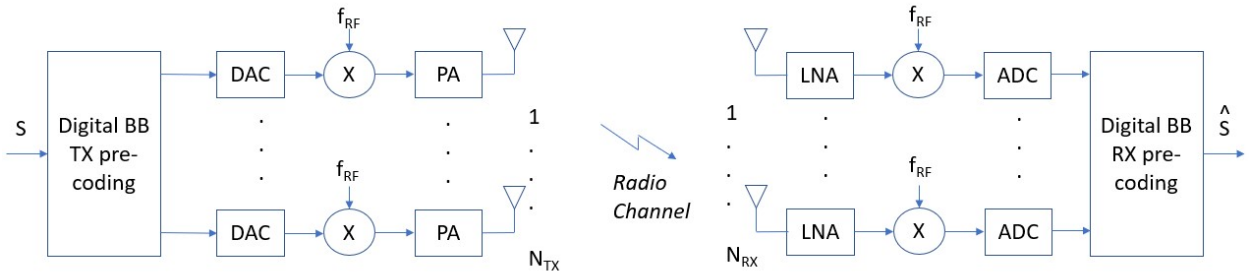


***Figure 4.*** *Digital beamforming radio architecture. The transmitted signal S is beamformed (pre-coded) for respective transmitter chain in the digital baseband prior to the DAC (left). At the receiver, the beamforming (pre-coding) is performed after the ADC in the digital baseband (right).*

# 5G mmWave in Mobile Devices - Current and Future Architectures

## Current Analog Beamforming Architecture

The 5G mmWave smartphones on the market 2020 are using analog beamforming. The solution is bulky and far from optimized with respect to cost, size and power consumption and therefore are more of a proof-of-concept implementation showing the benefits of mmWave communication. An example implementation of a first generation 5G mmWave mobile device is presented and discussed in [2] and [3]. The papers present an analog beamforming architecture implemented in a smartphone form factor (size 160x80 mm), with 8 antenna panels, each antenna panel consisting of 8 antenna elements each with a size of 25x18 mm(!), see figure 5, left hand side. Due to mmWave frequencies inability to penetrate solid material, holding on the antenna causes blocking of the radio signal. In order to mitigate that in handheld devices using analog beamforming architecture, one needs to implement multiple antenna panels in order to ensure that at least one antenna panel is free from blocking by the hand. A switching arrangement is needed for switching to an unobstructed antenna panel and hence, even if 8 antenna panels are totally implemented in the device, only 1-2 of them are actively used at the same time.

## Digital Beamforming Architectures – the Enabler of mmWave for the Mass Market

When mobile communication with mobile and IoT devices for the mass market now starts to target mmWave frequencies, the radio architecture really needs to be optimized from cost, size and performance perspective.

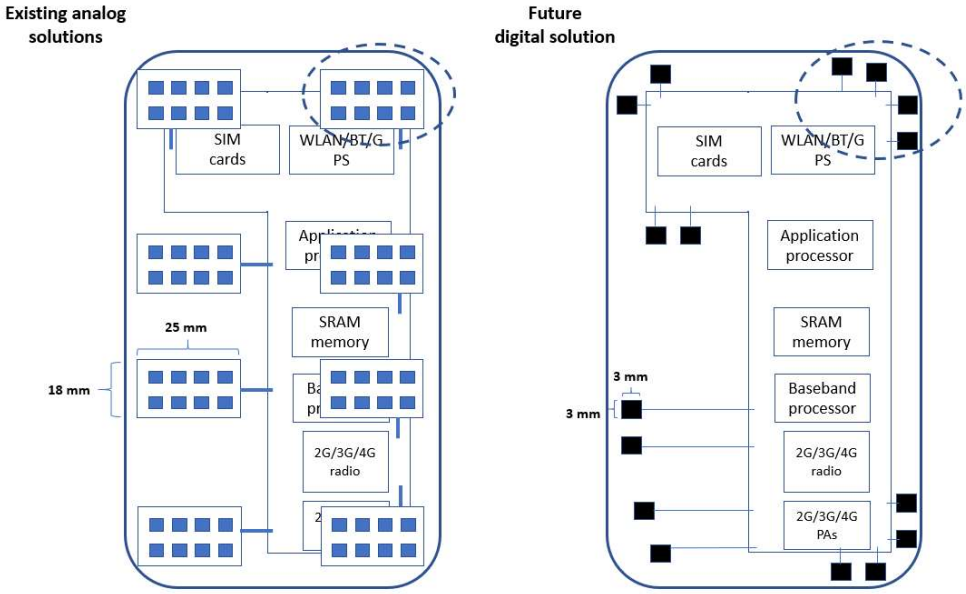


***Figure 5.*** *Analog Beamforming architecture, with 8 4x2 antenna panels of 25x18 mm² as described in [2] and [3] (left). A switching arrangement is used for switching to an unobstructed antenna panel, and hence, even if 64 antenna elements are totally implemented in the device, only 8-16 of them are actively used at the same time. Digital beamforming architecture where two antenna elements, front end modules, filters and RF IC are integrated in a single RF chip of 3 x 3 mm². 16 RF chips with in total 32 antenna elements (right). Total PCB size for digital beamforming architecture is 144 mm² compared to 3600 mm² for the analog beamforming architecture.*

The small antennas needed for mmWave open possibilities to ***integrate the RF IC, front end Radio modules, filters, and antenna element in a single RF chip***. This fact ***will drastically change the way beamforming will be implemented in mobile devices in the future***, ***since digital beamforming is more appropriate in this case.***

A single mmWave RF chip for digital beamforming, including RF IC, front end modules and filters as well as antenna elements will be in the size of 3 x 3 = 9 mm². Figure 5, right hand side, shows an example of digital beamforming architecture design, where two antenna elements are integrated in respective RF chips.

# Digital vs Analog Beamforming – A Power Consumption Analysis

Analog beamforming has been believed to be a more power efficient solution than digital beamforming for mmWave transceivers in mobile devices. This may have been the truth of yesterday, but – as will be shown in this section - with current state-of-the-art RF and AD/DA converter technologies, a digital beamforming solution as described above, has potential to achieve a power consumption on par or better than current analog versions.

In order to do the analysis, we need to go into details in the design solutions for the architectures shown in figure 5. We compare the power consumption for one 4x2 antenna panel (4 antennas for respective vertical and horizontal polarization) in current analog solution with the power consumption for a set of 4 RF chips with in total 8 antenna elements for the digital solution (vertical and horizontal polarization in respective chip), i.e. comparing the power consumption for respective radio components in the dashed areas in figure 5.

In the analog solutions [2] and [3], the antenna panel is connected to a single mmWave RF transceiver (or chip), which down/up-converts the mmWave radio signals to/from 3 GHz radio signals. The 3 GHz signals are then routed on the PCB and processed in an additional RF chip, which also handles 2G/3G/4G sub 6 GHz signals. In this sub 6 GHz RF chip the signals are down/up-converted to/from baseband signals and AD/DA converted. The input and output of the RF chip are digital baseband signals that are fed via a digital interface to the baseband processing unit for further signal processing, see figure 6 (left).

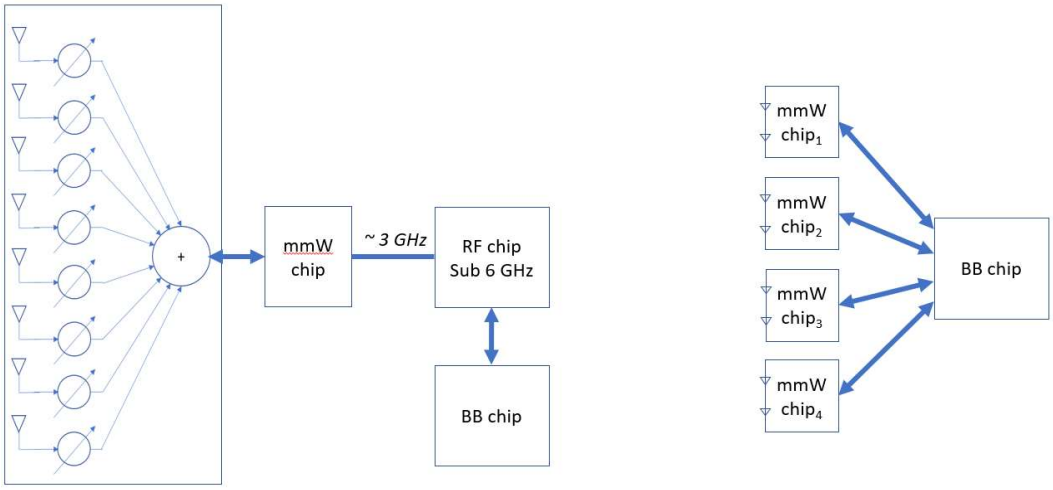


***Figure 6.*** *A principal sketch showing the analog beamforming solution according to [2] and [3] for a single 8 antenna array. The signal from the antenna panel is fed to a mmWave RF chip down-converting the mmW radio signal to a sub 6 GHz signal, and then fed into a sub 6 GHz RF chip down-converting the signal to a digital baseband signal (left). The digital beamforming solution comprises 4 mmWave RF chips with two integrated antennas and transceivers in respective chip, down-converting the mmWave radio signal directly down to a baseband signal and is then digitized (right). The interfaces towards the baseband chip is assumed to be digital in both solutions.*

In the digital solution, each RF chip comprises two antenna elements and two transceiver chains directly converting the mmWave radio signals to baseband signals, which are then AD/DA converted. From each RF chip the digital baseband signals are fed via a digital interface to the baseband processing unit for further signal processing, see figure 6 (right).

## Digital Beamforming requires fewer ADC/DAC bits than Analog Beamforming

ADC and DAC are typically quite power consuming, especially if high bit resolution is required. The digitalization of the signal introduces quantization noise and the Signal to Quantization Noise Ratio (SQNR) increases with approximately 6 dB per added bit [6]. For example, if the SQNR is required to be at least 45 dB, at least 8 bits ADC/DAC is required (since 7 bits only gives SQNR=42 dB), while if an SQNR of 36 dB is

required, 6 bits are sufficient. Furthermore, the ADC/DAC power consumption increases exponentially with the bit resolution, since it is proportional to $2^{nbit}$ [4], [5], [6]. Therefore, there is a significant advantage, in terms of ADC/DAC power consumption, if one can reduce the number of bits in the quantization.

An analog beamforming implementation has a power consumption advantage, by the need to only use one pair of ADC/DAC for the transceiver, compared to digital beamforming requiring $N_{antenna}$ pair of ADC/DACs, one pair for each antenna branch.

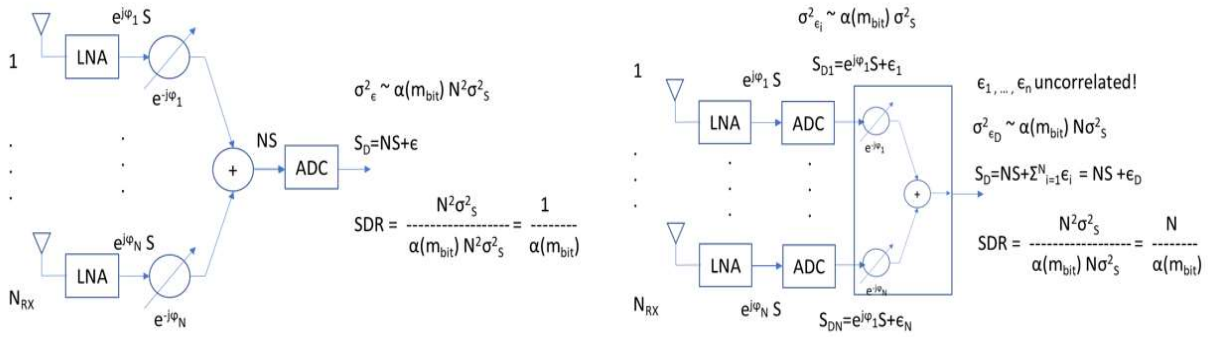


***Figure 7.*** *Example showing the ADC quantization noise suppression in analog and digital beamforming architectures. For simplifying we assume the random radio channel at antenna i is only a complex-valued phase shift $e^{\varphi(i)t}$ of the wanted signal S, with signal power $\sigma^2_S$. In the analog beamforming case (left), the phase is compensated and combined prior to the ADC, and the quantization noise power $\sigma^2_\epsilon$, of the input signal N*S, assuming $m_{bit}$ bits ADC is proportional to $\alpha(m_{bit})N^2\sigma^2_S$. Hence the SQNR will be a function of $1/\alpha(m_{bit})$, or approximately $6*m_{bit}$ dB. In the digital beamforming case (right), however, the signal is quantized per antenna branch prior to the phase compensation and combing of signal. Therefore, the quantization noise power $\sigma^2_\epsilon$ is proportional to $\alpha(m_{bit})\sigma^2_S$ in this case, and utilizing that the noise $\epsilon_i$ is uncorrelated between the antenna branches, the noise power of the combined signal $\sigma^2_{\epsilon D}$ is $\alpha(m_{bit})N\sigma^2_S$. Hence the digital beamformer SQNR is $N/\alpha(m_{bit})$, or approximately $6*m_{bit} + 10log_{10}(N)$ dB.*

However, the $N_{antenna}$ number of ADC/DAC in a digital beamforming architecture requires approximately $1.7log_{10}(N_{antenna})$ fewer bits compared to the single ADC/DAC needed in an analog beamforming architecture. The reason for this exemplifying the receiver case, disclosed in figure 7, is that in a digital beamforming architecture, the quantization noise is added on respective receiver chain, and then in the digitally combiner, that *coherently combines the signal* from respective antenna, while the *quantization noise, that is uncorrelated, is non-coherently combined*, and therefore quantization noise suppression of a factor $N_{antenna}$ is achieved. In the analog beamforming architecture, the signal is *combined before* the ADC and hence there is *no such quantization noise interference suppression*. The same arguments hold for the transmitter chain and DAC case as well.

Hence, for achieving the same SQNR, $10log_{10}(N_{antenna})/6 \approx 1.7log_{10}(N_{antenna})$ fewer bits can be used in ADC/DAC:s for the digital beamformer compared to the analog beamformer, and in our further analysis where $N_{antenna}$=8, we assume that the digital beamforming architecture uses 2 bits less in the ADC and DAC compared to the analog beamforming solution.

## Power Consumption Analysis Approach

The analysis below follows the approach described in [4] and [5]. As mentioned above, we compare the power consumption for one 4x2 antenna panel in current analog solution with the power consumption for a set of 4 RF chips with in total 8 antenna elements for the digital solution. The power consumption for each radio component is estimated by using the current state-of-the-art of numbers found in [4]-[8}. The frequency band is 28 GHz and a system bandwidth of 200 MHz is assumed, a typical system bandwidth for 5G-NR in the mmWave frequency band. A power class 3 [1] mobile device is assumed and the received signal level is in the analysis determined to be at the 3GPP reference sensitivity of -82 dBm. For the transmitter, a transmitter power of 9 dBm from each antenna is assumed, and using 4 antennas for respective vertical and horizontal polarization and assuming an antenna gain of around 5 dBi per antenna, giving a total EIRP TX power of approximately 26 dBm.

Figure 8 shows a more detailed block diagram of the analog beamforming architecture as assumed in [2] and [3], while figure 9 shows the corresponding block diagram for the digital beamforming architecture for a single mmW chip as disclosed in figure 6 (right).

## Front-end Transceiver

The transceiver front end comprises Power Amplifiers (PA), Low Noise Amplifiers (LNA), mixers, Local Oscillators (LO), as well as - for analog beamforming - phase shifter and power combiners/splitters. The phase shifters, power combiners and mixers are assumed to be passive components which introduces insertion loss (IL) but not draw any power. Typical IL for passive mixers is $IL_{mixer}$=6 dB, while the IL for phase shifters and power combiner and power splitters is $IL_{PS}$ = 8 dB, see [5], [8]. Furthermore, the power consumption for the Local Oscillators (LO) is based on [7] and is assumed to be 30 mW, in the analog case, and 40 mW for the digital solution for two the two LO: s generated in the chip. In case of two LO: s in a single chip, parts of the designs can be reused between the two transceiver chains and therefore the power consumption is not doubled.

Following the principles in [5], for the analog case we assume the input power to the up-conversion mixer in the mmWave RF chip is 5 dBm. In the digital solution, the input power to the mixer is assumed to be -4 dBm per branch. The 6 dB mixer IL gives input of -10 dBm into the PA in the digital case, while in the analog case, with the 1:8 power splitter and the IL from mixers splitter and phase shifters, the input power to the respective PA is -18 dBm. The output from the respective PA is 9 dBm and with a power efficiency of 15% that includes also losses in front-end RX-TX switches etc. we end up in 417 mW for the analog beamformer PA part, while in the digital case the PAs consumes 103 mW per chip.

The main power contributor in the front-end receiver is the LNA, that are characterized by their Figure of Merit (FoM) which relates the gain G and the noise figure N to the power consumption as $P_{LNA}= G_{LNA}/\{FoM*(N_{LNA}-1)\}$, see for instance [4], [5]. Now, if the LNA gain is selected as $G_{LNA,dig}$ for the digital beamformer, the required LNA for the analog beamformer will be $G_{LNA,ana}$ = ($G_{LNA,dig}$ + $IL_{PS}$) which compensates for the insertion loss due to the phase shifters and power combiner. Using the state of-the-art LNA referred to in [5], with $N_{LNA}$ =3.2 dB and $G_{LNA,dig}$=17 dB, giving $G_{LNA,ana}$ = 25 dB, and LNA FoM=8.12 $mW^{-1}$ , a total analog beamforming LNA power consumption of 286 mW is achieved, while a power consumption of 11.3 mW per chip is achieved in the digital beamforming case. As can be noted, the extra

gain needed in the analog beamformer LNAs for compensation of the insertion loss in the analog phase shifters significantly increases the power consumption compared to a digital solution.

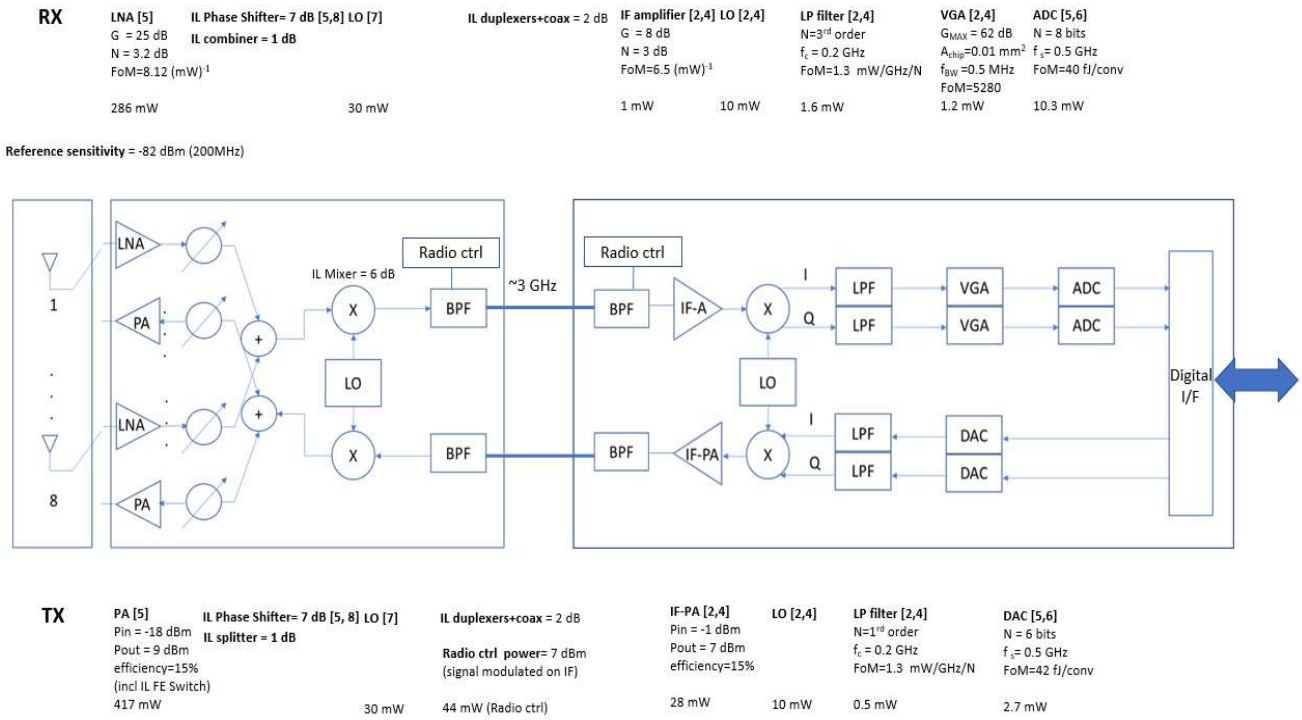


***Figure 8.*** *Analog beamforming super-heterodyne architecture assuming an 8-antenna array according to [2] and [3]. The Figure of Merit (FoM) for respective radio components originates from the references [2]-[8] and the power consumption estimates are based on these FoM.*

## IF-part of the Analog Beamforming

Since the analog beamforming architecture is super-heterodyne [2], there are some additional radio components required compared to the digital solution. The connection between the mmWave chip and the sub 6 GHz radio chip is over a coaxial cable, and an insertion loss in the cable together with the 3 GHz band pass filters (BPF) can be estimated to be 2 dB. The Intermediate Frequency (IF) PA as well as the IF amplifier on the receiver side is designed to compensate for the IL in the coaxial cable as well as the 6 dB IL in the passive IF mixer. The IF PA output power is then 7 dBm, with an input power of -1 dBm. Assuming 15% efficiency, the IF-PA power will be 28 mW. The IF amplifier only needs to compensate for 8 dB loss, and assuming a FoM from [4], the power consumption will be in the single mW range. The LO down-converting the 3 GHz signal to a baseband signal can be designed with lower power consumption than a mmW LO, and it is assumed to consume 10 mW [4]. Finally, there is a need for a radio control unit for

control signaling between the chip that can be modulated on the 3 GHz carrier in the coaxial cable, as described in [2], [3]. The radio control signaling is assumed to be output with power 7 dBm and together with other processing of the radio control signaling, it is assumed to consume a total of 44 mW.

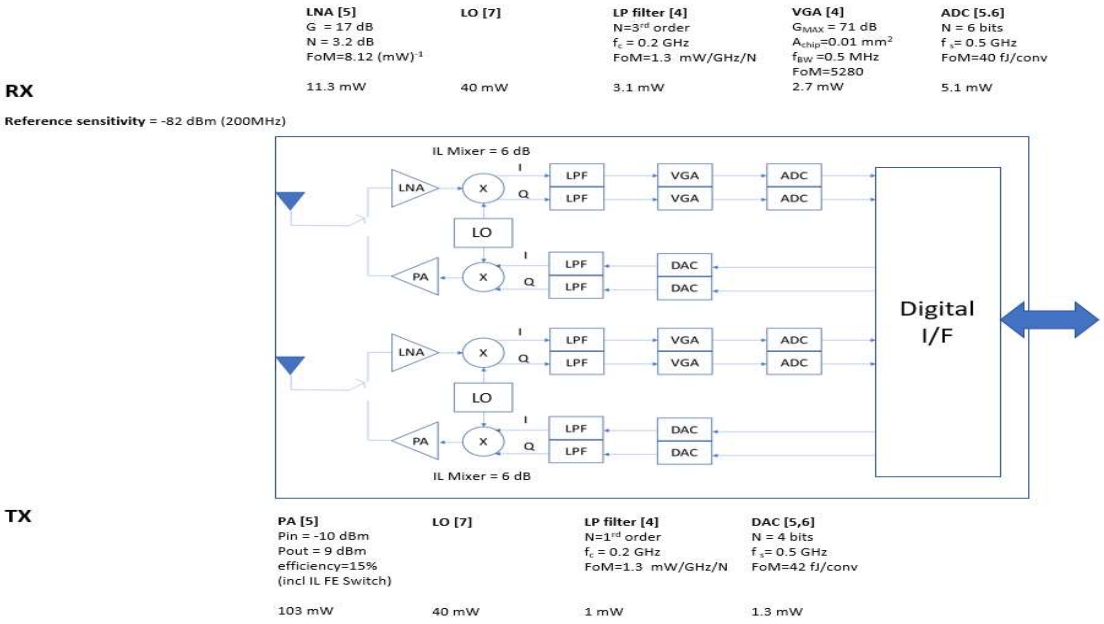


***Figure 9.*** *A Digital beamforming architecture where the RF IC, front end radio modules, filters, and antenna element for two transceiver chains are integrated in a single RF chip. The Figure of Merit (FoM) for respective radio components originates from the references [2]-[7] and the power consumption estimates are based on these FoM. Note that the power consumption numbers are for a single RF chip, i.e. two transceiver branches.*

## ADC/DAC

Now, focusing on the baseband radio part. The power consumed for DAC as well as ADC ($P_{conv}$) is a linear function of the sampling frequency $f_s$ and grows exponential with the number of bits of resolution ($n_{bits}$) as, $P_{conv} = FoM_{conv} * f_s * 2^{nbits}$, where $FoM_{conv}$ is the Figure of Merit of the converter. In the case studied in this paper, we assume a signal bandwidth of 200 MHz, and a converter sample rate of $f_s = 500$ MHz. In the simulation studies of digital beamforming architectures in [4] and [5] they concluded that a 4 bits DAC in combination with a first order transmitter low-pass (LP) filter was sufficient to fulfill 3GPP adjacent channel leakage requirements, so in our analysis we assume a 4 bits DAC for the digital solution. From the discussion above, we know that we can use 2 bits less in a digital beamformer compared to an analog beamformer in case we have 8 antenna branches for achieving the same SQNR w.r.t quantization noise. Hence, for the analog beamforming architecture we assume a 6 bits DAC.

For the receiver part, the simulation studies in [4] and [5] also indicated that a 4 bits ADC was sufficient. However, in order to make room for adjacent channel and out-of-band blocking for fulfilling the 3GPP requirements [1] as well as a non-ideal- Automatic Gain Control, (AGC), we assume a need for two bits

extra and therefore, a 6 bits ADC is assumed in the digital case, and an 8 bits ADC for the analog solution. From [5] and [6] we can find converters with $FoM_{conv}$ =42 fj/conv (DAC), and $FoM_{conv}$ = 40 fj/conv (ADC), giving 10.3/2.7 mW for the ADC/DAC for analog beamforming, and 5.1/1.3 mW per chip for the ADC/DAC for digital beamforming.

### Transceiver LP-filters

According to [5] the power consumption for active low pass filters can be determined as $P_{LP}= FoM_{LP} * f_c*N$, where $f_c$ = 200 MHz, N is the LP filter order, and $FoM_{LP}$ = 1.3 mW/GHz/N. For the transmitter side, N=1, as determined, in [4],[5], sufficient for fulfilling 3GPP requirements, while for the receiver side a 3$^{rd}$ order filter is assumed, allowing for sharper filtering of possible strong adjacent channel and out-of-band blocking signals. The Power consumption is 1.6 (RX)/0.5(TX) mW for analog beamforming, and 3.1 (RX)/1 (TX)mW per chip for the digital beamforming case.

### Receiver VGA

Finally, to maintain a constant baseband power into the ADC, a Variable Gain Amplifier (VGA) at the input of the ADC is needed. The power consumption is highest for the highest gain, that is determined based on the reference sensitivity requirement, -82 dBm in the 200 MHz BW case, and wanted input into the ADC, that is assumed to be 0 dBm. The maximum gain for the digital solution is then $G_{VGA,dig}=82-G_{LNA,\ dig}+IL_{mixer}$ =71 dB. Similarly, the maximum gain for the analog VGA is $G_{VGA,ana}=82-G_{LNA,ana}+IL_{PS}-10log10(N_{ant})+IL_{mixer}$=62 dB. The power consumption for the VGA is determined by $P_{VGA}=(G_{VGA} * f_{BW})/(FoM_{VGA} * A_{chip})$, where $f_{BW}$=0.5 GHz, $A_{chip}$=0.01 mm$^2$, and $FoM_{VGA}$ = 5280, see [4] and [5], giving 1.2 mW for the analog case, and 2.7 mW per chip for the digital case.

Table 1 shows a summary of the power consumption estimates, where the numbers for the digital solution has been multiplied with 4 to mirror the usage of 4 mmW RF chip to get an 8-antenna solution comparison, as disclosed in figure 6 (right).

For the transmitter part, the analog beamforming has lower power consumption, 532 vs 581 mW for the digital solution, however for the receiver part, the digital beamforming architecture has the lowest power consumption, 249 vs 340 mW for analog beamforming. In practical mobile device use cases, there is an asymmetry in the uplink and downlink usage. In the paper [9] the uplink/downlink asymmetry was analyzed for smartphone usages in real networks, showing a ratio of around 2-2.3 between downlink data and uplink data. This number is typically mirrored on the usage of DL vs UL time slots in TDD and hence as a KPI for typical power consumption one should average the power consumption assuming a 70% downlink, 30% uplink usage ratio. Doing that, one can see in Table 1 that ***digital beamforming is the most power efficient architecture for mobile devices with an average power of 349 mW compared to 398 mW for the analog solution.***

## Take-away

The optimal way to perform beamforming for mmWave radio frequencies, in terms of performance, cost, size, and flexibility from a PCB design point of view to is to use a digital beamforming architecture (as discussed in [10]).

***Table 1:*** *Power Consumption comparison, for a typical mmWave use case, between a mobile device digital and analog beamforming architecture assuming 8 antennas respectively. For the TX part, the analog beamforming has lower power consumption, 532 vs 581 mW, however for the receiver part, the digital beamforming architecture has the lowest power consumption, 249 vs 340 mW. The reason for this is twofold. First, the insertion loss in the phase shifters and power combiners/splitters in the front-end radio increases the front-end power consumption for analog beamforming. Second, the digital beamforming requires 1.7log10(Nantenna) fewer bits in the converters, due to the inherent quantization noise suppression ability in the digital beamforming architecture, thereby reducing the ADC/DAC power consumption for the digital solution. Assuming a 70% downlink, 30% uplink slot allocation, according to typical smartphone DL/UL data usage asymmetry [9], the digital beamforming is the most power efficient architecture for mobile devices with an average power of 349 mW compared to 398 mW for the analog solution.*

| **Component** | **Digital BF Architecture [mW]** | **Ref Analog BF Architecture, [3] [mW]** |
|---|---|---|
| D/A converter | 5.2 | 2.7 |
| TX LP-filter | 4 | 0.5 |
| TX IF radio | - | 38 |
| Front end TX | 572 | 447 |
| IF Radio Ctrl | - | 44 |
| **Total TX power consumption** | **581** | **532** |
| A/D Converter | 20.4 | 10.3 |
| VGA | 10.8 | 1.2 |
| RX LP-filter | 12.4 | 1.6 |
| RX IF | - | 11 |
| Front end RX | 205 | 316 |
| **Total RX power consumption** | **249** | **340** |
| **Average Power Consumption (70% DL, 30% UL) [8]** | **349** | **398** |

Furthermore, from this paper we can conclude that with current state of the art RF and AD/DA converter technologies, the power consumption for a digital beamforming architecture, when integrating antennas, front-end filters and radio transceiver in a single RF Chip, is at least on par and in a typical use case of 70% downlink data and 30% uplink data, lower than the corresponding power consumption for analog beamforming architectures currently implemented in mmWave 5G mobile devices.

The reason for this is twofold. First, the insertion loss in the phase shifters and power combiners and power splitters in the front-end radio making the PA and LNA having higher power consumption for an analog beamforming architecture compared to the digital architecture, where no such components are needed. Second, the digital beamforming requires fewer bits in the converters, due to the inherent quantization noise suppression ability in the digital beamforming architecture, thereby reducing the ADC/DAC power consumption.

The take away from this paper is that a digital beamforming architecture where the RF IC, front end radio modules, filters, and antenna element are integrated in a single RF chip represents the radio architecture that will enable the mass market for 5G-NR devices on mmWave radio frequencies.

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